UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/803,047	03/18/2004	Der-Zheng Liu	REAP0463USA	4615

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EXAMINER
PERILLA, JASON M

ART UNIT	PAPER NUMBER
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NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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PTOL-90A (Rev. 04/07)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-10,12,15,16 and 18-23* is/are pending in the application.

    4a) Of the above claim(s) *5,15,21 and 22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,5-10,12,15,16 and 18-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All   b)☐ Some * c)☐ None of:

      1.☒ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

   * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____ .

DETAILED ACTION

1.   Claims 1-3, 5-10, 12, 15, 16, and 18-23 are pending in the instant application.

Claims 5, 15, 21, 22 are withdrawn.

Response to Amendment/Argument

2.   The Applicant's arguments, filed March 17, 2008, have been considered in light

of the accompanying amendments to the claims.

In view of the Applicant's amendments to the claims, new rejections under 35

U.S.C. § 112, first paragraph, have are applied below.

In view of the Applicant's amendments to the claims, new prior art rejections are

set forth below.

Claim Rejections - 35 USC § 112

3.   Claims 1-3, 5-10, 12, 15, 16, and 18-23 are rejected under 35 U.S.C. § 112, first

paragraph, as failing to comply with the written description requirement. The claim(s)

contains subject matter which was not described in the specification in such a way as to

reasonably convey to one skilled in the relevant art that the inventor(s), at the time the

application was filed, had possession of the claimed invention.

Regarding claim 1, the claim is rejected because the new limitation of calculating

a "subtraction" between first and second differences of frequency responses is

considered to be new matter. At most, the specification discloses that a "difference"

between them is determined. In as much as a calculating a "subtraction" is more

limiting than calculating a "difference", the amendment to the claim presents new

matter. Nowhere in the speciation, claims, or drawings of the instant application was a

"subtraction" between first and second differences of frequency responses specifically disclosed in the originally filed application, and, as specifically as claimed, it is considered to be new matter.

Regarding claims 2, 3, and 6-9, the claims are rejected as being based upon a rejected parent claim.

Regarding claim 10, the claim is rejected for the same reasons as applied to claim 1 above.

Regarding claims 12, and 16, the claims are rejected as being based upon a rejected parent claim.

Regarding claim 18, the claim is rejected for the same reasons as applied to claim 1 above.

Regarding claims 19, and 20, the claims are rejected as being based upon a rejected parent claim.

Regarding claim 23, the claim is rejected for the same reasons as applied to claim 1 above.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5.   Claims 1-3 are rejected under 35 U.S.C. § 103(a) as being unpatentable over

Imamura (U.S. Pat. No. 6862262 – previously cited) in view of Ito et al (U.S. Pub. No.

2003/0128660).

Regarding claim 1, Imamura discloses an apparatus for sampling timing

compensation at a receiver of a communication system (abstract; fig. 3), wherein each

of at least two pilot signals (fig. 2) comprises a first pilot signal and a second pilot signal

(fig. 2; i.e. first and second "CHANNEL ESTIMATION PILOT SYMBOL"), the pilot

signals transmitted via respective pilot subchannels (i.e. "each pilot carrier"; col. 6, line

10) and the first and the second pilot subchannels comprising a first and a second pilot

indexes (see "A" below) respectively, the apparatus comprising: a pilot subchannel

estimator (fig. 3, refs. 103 and 104) for generating frequency responses (fig. 3, ref. 103)

of each of the first and second pilot signals (col. 5, line 50) of each pilot signal of each

subchannel (col. 5, lines 40-60); a timing offset estimator (fig. 3, ref. 104 illustrated as

figs. 4 and 5, ref. 204), coupled to the pilot subchannel estimator (fig. 3, ref. 103), for

calculating a timing offset according to a first difference (col. 5, line 48; "differential

detection") between the first and second pilots signals of the first subchannel pilot

signal, a second difference between the first and second pilot signals of the second

subchannel pilot signal ("of each pilot carrier output"; col. 6, line 9) and a "difference"

between the first and second differences (col. 6, lines 5-15); and a phase rotator (fig. 4,

ref. 209), coupled to the timing offset estimator, for performing sampling timing

compensation according to a phase rotation corresponding to the timing offset.

Imamura discloses an apparatus for correcting sampling in an OFDM receiver (fig. 3)

which utilizes pilot symbols in each of a plurality of pilot subchannels. Regarding

limitation "A" above, as broadly as claimed, each OFDM subchannel of Imamura

comprises a separate and distinct "index" or identifier because each is a separate and

distinct subchannel. Imamura determines a phase difference between a first and

second pilot signals of each of a plurality of pilot subchannel pilot signals in the phase

error calculation unit (fig. 4, ref. 204). Imamura further discloses adders (fig. 5, refs. 301

and 302) provided to "add up all differential detection (phase error) outputs of each pilot

carrier output" (col. 6, lines 5-10). After summing the phase errors, the accumulated

phase error is normalized (fig. 5, refs. 305 and 306; col. 6, lines 18-22) to determine the

timing offset using a memory (fig. 4, ref. 206). As broadly as claimed, Imamura

discloses that the timing offset is determined, indirectly, according to "a difference

between the first and second differences" because the magnitude of the difference

between the first and second differences is captured in the normalized output of the

phase error calculation unit (fig. 4, ref. 204). Imamura discloses determining "a

difference between the first and second differences" of pilot signal frequency responses

but does not explicitly disclose "subtracting" a difference between the first and second

differences. However, the use of a subtractor to subtract frequency responses among

various pilot signals is well known in the art as evidenced by Ito. Ito discloses, in strictly

analogous art, a subtractor (fig. 9, ref. 801) which subtracts phase deviations (i.e. a

frequency response) between various pilot signals (¶ 0201) to aide in the determination

of an accurate phase deviation result. Therefore, it would have been obvious to one

having ordinary skill in the art at the time which the invention was made that the

difference determining normalizer of Imamura could be modified to directly determine a

subtraction result between differences between pilot signal frequency responses of

more than one subchannel because it is a well known and accepted method of

determining offsets for reducing sampling timing error which produces only expected

and routine results.

Regarding claim 2, Imamura in view of Ito disclose the limitations of claim 1 as

applied above. Further, Imamura discloses that the communication system is a multi-

carrier "OFDM" system (abstract).

Regarding claim 3, Imamura in view of Ito disclose the limitations of claim 1 as

applied above. Further, Imamura discloses that the timing offset estimator further

comprises a phase difference calculating device (fig. 5, refs. 301-304) for calculating a

phase difference between the first and second frequency responses and a divider (fig.

5, refs. 305 and 306) for calculating the timing offset according to the phase difference

and a difference between the first and second pilot indexes (col. 5, line 30 – col. 6, line

40). The pilot indexes are determined according to their position in time. Hence, "the

time elapsed between the two data symbols" is associated with the pilot indexes.

6.   Claims 6, 10-12, 16, 18, 19, 20, and 23 are rejected under 35 U.S.C. § 103(a) as

being unpatentable over Imamura in view of Ito and Singh et al (U.S. Pat. No. 7139320;

"Singh" – previously cited).

Regarding claim 6, Imamura in view of Ito disclose the limitations of claim 1 as

applied above. Further, Imamura discloses determining a phase difference between the

pilot symbols of many subcarriers of a multicarrier system as applied to claim 1 above.

(Such difference is indicative of a frequency offset between the transmitter and the

receiver.) However, although one skilled in the art is aware that such offset is

manifested in the receiver due to poor synchronization of the receiver's local oscillation

and sampling frequencies (i.e. Imamura fig. 3, ref. 102; col. 4, lines 10-20) with respect

to the operating frequency of the transmitter, Imamura does not explicitly disclose the

correction of a sampling frequency offset. However, Singh discloses, in a strictly

analogous sampling timing compensation apparatus (fig. 4), compensating both the

downconverter frequency (fig. 4, ref. 32) and sampling timing frequency (fig. 4, ref. 34;

col. 8, lines 45-55) according to the determined pilot offset (col. 8, lines 15-35). Singh's

compensation is performed for frequency synchronization between the OFDM

transmitter and receiver (col. 8, lines 52-55). Therefore, it would have been obvious at

the time the invention was made that Imamura's (i.e. Imamura in view of Ito)

determination of phase offset could be advantageously utilized to update the

downconverter and sampling frequencies (Imamura; fig. 3, ref. 102) as taught by Singh

because it would achieve frequency synchronization between the OFDM transmitter and

receiver. Further, Singh discloses a timing controller (fig. 4, output of 80) for generating

a control signal ("FREQUENCY SYNCH ADJUSTMENT") according to the timing offset,

wherein the phase of the sampling clock (fig. 4, ref. 82) is adjusted according to the

control signal; and an analog-to-digital converter (ADC) (fig. 4, ref. 34) for converting the

symbol according to the sampling clock. These items correspond to the

downconverting and sampling (fig. 3, ref. 102) of Imamura (col. 4, lines 10-20).

Regarding claim 10, Imamura in view of Ito and Singh disclose the limitations of the claim as applied to claim 6 above.

Regarding claim 11, Imamura in view of Ito and Singh disclose the limitations of claim 10 as applied above. Further Imamura in view of Singh disclose the remaining limitations of the claim as applied to claim 3 above.

Regarding claim 12, Imamura in view of Ito and Singh disclose the limitations of claim 11 as applied above. Further Imamura in view of Singh disclose the remaining limitations of the claim as applied to claim 3 above.

Regarding claim 16, Imamura in view of Ito and Singh disclose the limitations of claim 10 as applied above. Further Imamura in view of Singh disclose the remaining limitations of the claim as applied to claim 6 above.

Regarding claim 18, Imamura in view of Ito and Singh disclose the limitations of the claim as applied to claim 6 above. Further Imamura in view of Nakahara and Singh disclose a pre-FFT processing device for processing in the time domain (Imamura; fig. 3, ref. 102), a FFT for transforming the symbols to the frequency domain (Imamura; fig. 3, ref. 103), and a, adjusting device for adjusting the operation of the pre-FFT processing device (Singh; fig. 4, refs. 80 and 82).

Regarding claim 19, Imamura in view of Ito and Singh disclose the limitations of claim 18 as applied above. Further, Imamura discloses that the pre-FFT processing device includes an ADC as applied in claim 18 above.

Regarding claim 20, Imamura in view of Ito and Singh disclose the limitations of claim 19 as applied above. Further, Imamura discloses that the pre-FFT processing

device further includes a timing controller (fig. 4, output of 80) for generating a control signal ("FREQUENCY SYNCH ADJUSTMENT") according to the timing offset and a clock generator (fig. 4, ref. 82) for controlling the operation of the ADC (fig. 4, ref. 34).

Regarding claim 23, Imamura in view of Ito and Singh disclose the limitations of the claim as applied to claim 6 above.

7.   Claims 7, 8, and 17 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Imamura in view of Itoa, Singh, and National ("Application of the ADC1210 CMOS A/D Converter"; National Semiconductor Application Note 245, April 1986 – previously cited).

Regarding claim 7, Imamura in view of Ito and Singh disclose the limitations of claim 6 as applied above. Imamura in view of Ito and Singh do not explicitly disclose that the period of the sampling clock (Tf) is shorter than a sampling interval (Ts) of the ADC. However, it is notoriously known in the art that many modern ADC converters require multiple clock periods to convert an analog signal into a high resolution binary number. Such ADC converters operate in a type of serial fashion to save cost. Specifically, National discloses, on the second column of page 5, that a 500kHz clock could be utilized by the disclosed ADC to create a 12 bit digital representation of an analog signal in 26us. That is, the period of the sampling clock (a 500kHz clock has a 2us period) is more frequent (shorter) than the sampling output interval (every 26us). Therefore, it would have been obvious to one having ordinary skill in the art at the time which the invention was made to utilize a serial fashion output ADC converter as

disclosed by National having a longer sampling interval than sampling clock interval in

the apparatus of Imamura in view of Nakahara and Singh because it would save cost.

Regarding claim 8, Imamura in view of Ito, Singh, and National disclose the

limitations of claim 7 as applied above. Further, Imamura in view of Ito, Singh, and

National disclose the remaining limitations of the claim as applied in claim 7 above.

Regarding claim 17, Imamura in view of Ito and Singh disclose the limitations of

claim 13 as applied above. Further Imamura in view of Ito, Singh, and National disclose

the remaining limitations of the claim as applied to claim 7 above.

8.   Claim 9 is rejected under 35 U.S.C. § 103(a) as being unpatentable over

Imamura in view of Ito, Singh, and Matheus et al (U.S. Pat. No. 7009932; hereafter

"Matheus" – previously cited).

Regarding claim 9, Imamura in view of Ito and Singh disclose the limitations of

claim 6 as applied above. Imamura in view of Ito and Singh do not disclose, however,

that the clock generator (Singh; fig. 4, ref. 82) comprises a PLL. Rather, Singh

illustrates and discloses a Numerically Controlled Oscillator (NCO). However, the use

of phase locked loop circuits as oscillators is notoriously known in the art as taught and

disclosed by Matheus (fig. 5, ref. "CORR1"; col. 15, lines 10-12). Therefore, it would

have been obvious to one having ordinary skill in the art at the time that the invention

was made to utilize a PLL in place of Singh's NCO to generate a clock signal because

the use of a PLL is well known and accepted in the art.

Conclusion

9.   Applicant's amendment necessitated the new ground(s) of rejection presented in

this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP §

706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR

1.136(a).

        A shortened statutory period for reply to this final action is set to expire THREE

MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later

than SIX MONTHS from the date of this final action.

10.   Any inquiry concerning this communication or earlier communications from the

examiner should be directed to JASON M. PERILLA whose telephone number is

(571)272-3055. The examiner can normally be reached on M-F 8-5 EST.

        If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Chieh M. Fan can be reached on (571) 272-3042. The fax phone number

for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

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system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jason M Perilla/
Art Unit 2611
August 6, 2008

/jmp/

/Chieh M Fan/

Supervisory Patent Examiner, Art Unit 2611